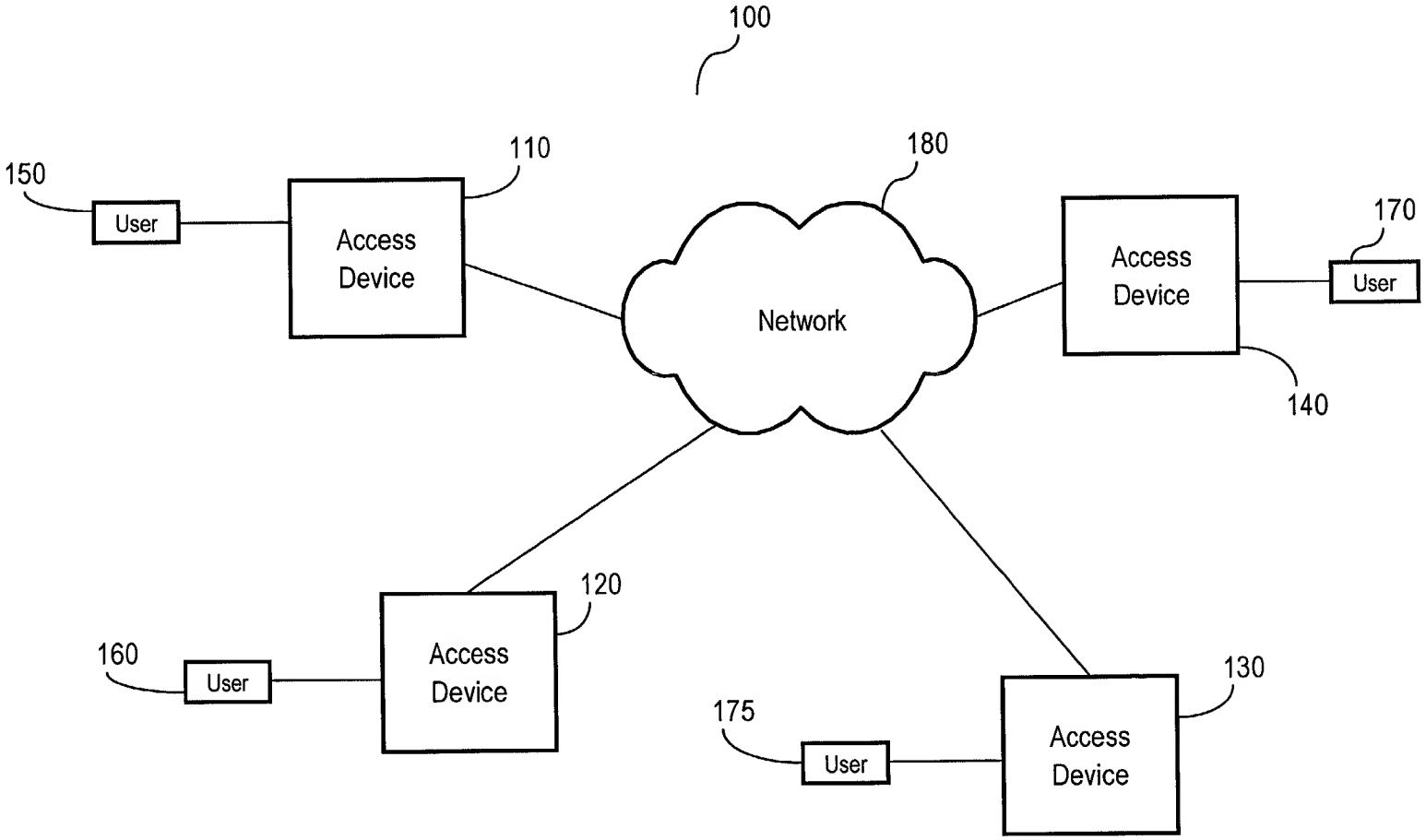
Fig. 1


100
150
User
110
Access Device
180
Network
170
Access Device
User
140
160
User
120
Access Device
175
User
130
Access Device

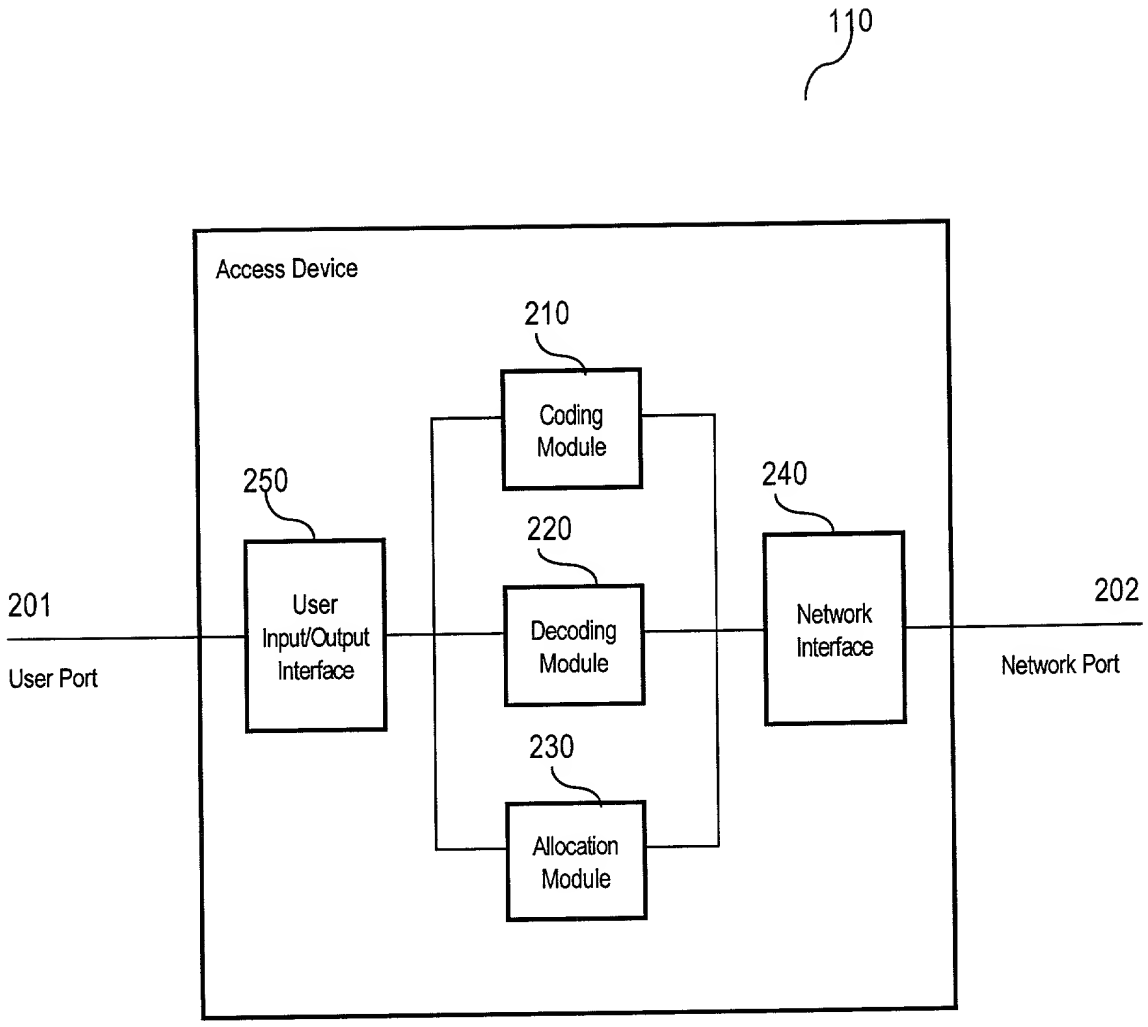

110
Access Device
210
Coding Module
250
240
220
201
User Input/Output Interface
Decoding Module
Network Interface
202
User Port
Network Port
230
Allocation Module

Fig. 2

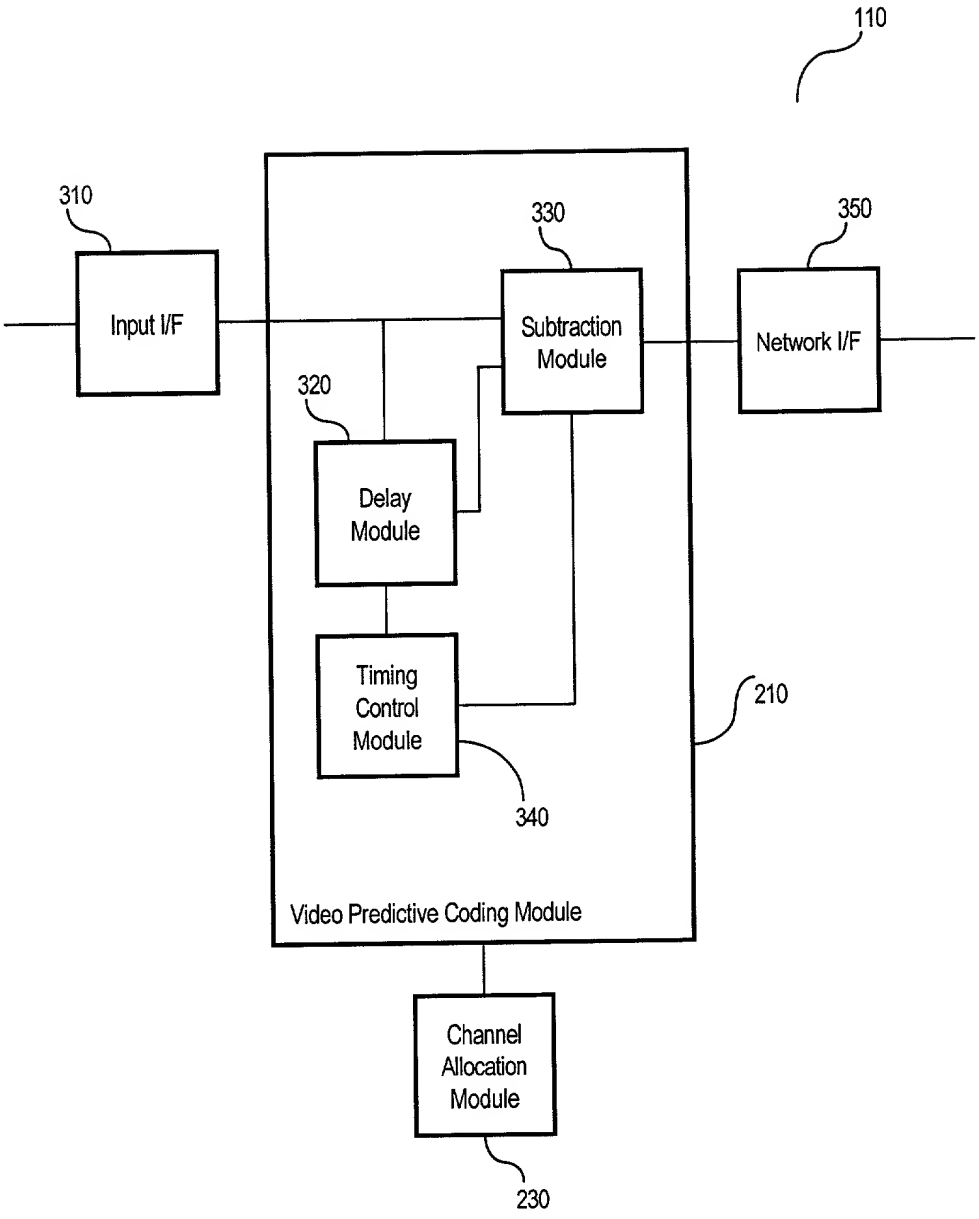

110
310
330
350
Input I/F
Subtraction Module
Network I/F
320
Delay Module
Timing Control Module
210
340
Video Predictive Coding Module
Channel Allocation Module
230

Fig. 3

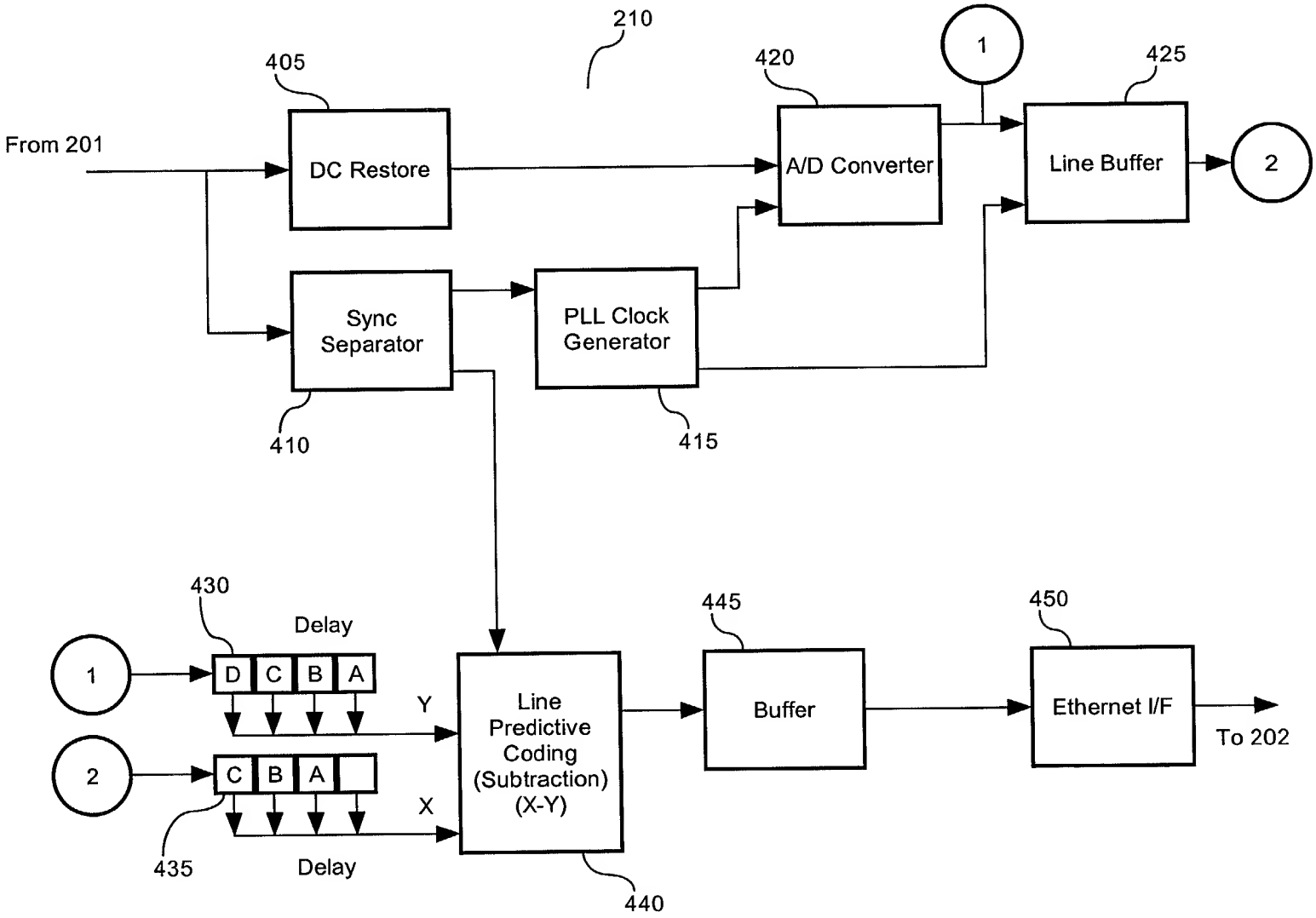

210
405
420
1
425
From 201
DC Restore
A/D Converter
Line Buffer
2
Sync Separator
PLL Clock Generator
410
415
430
Delay
445
450
1
D C B A
Y
Line Predictive Coding (Subtraction) (X-Y)
Buffer
Ethernet I/F
To 202
2
C B A
X
435
Delay
440

Fig. 4

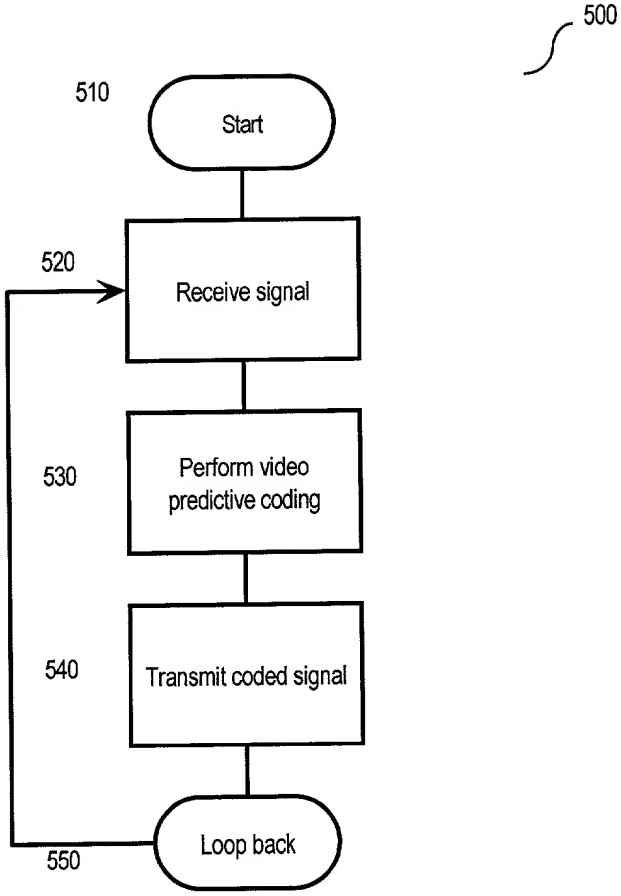

500
510
Start
520
Receive signal
530
Perform video predictive coding
540
Transmit coded signal
550
Loop back

Fig. 5

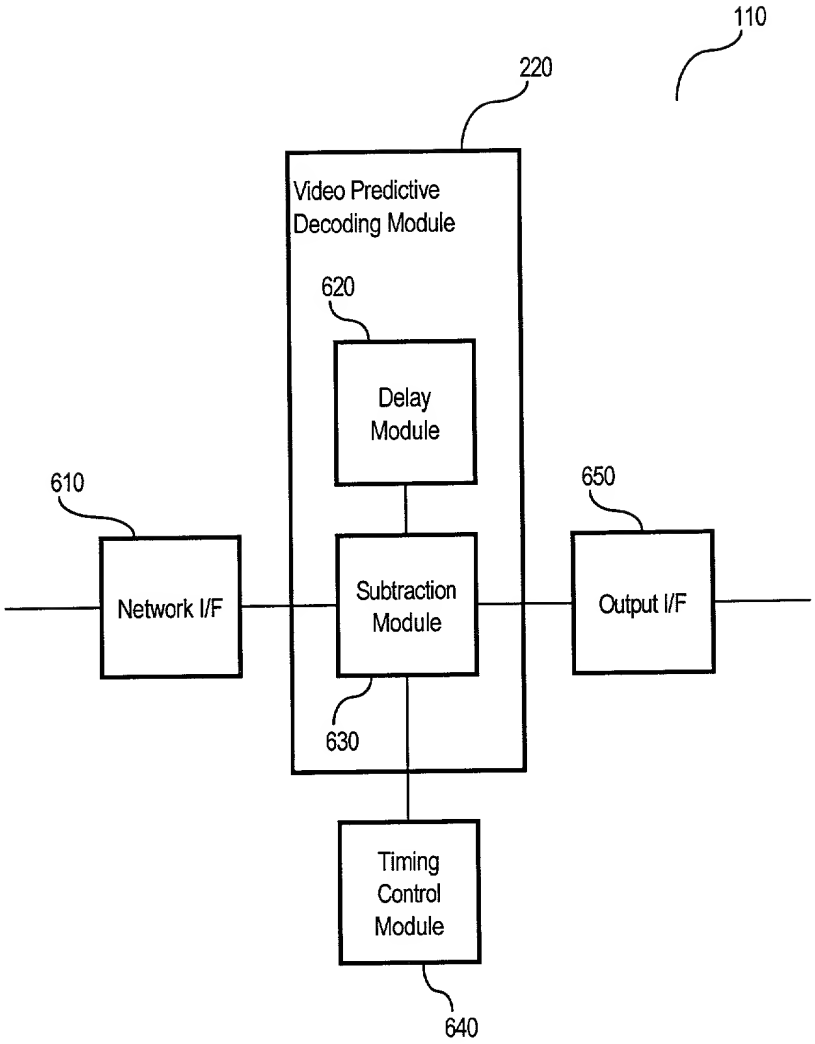

110
220
Video Predictive
Decoding Module
620
Delay
Module
610
650
Network I/F
Subtraction
Module
Output I/F
630
Timing
Control
Module
640

Fig. 6

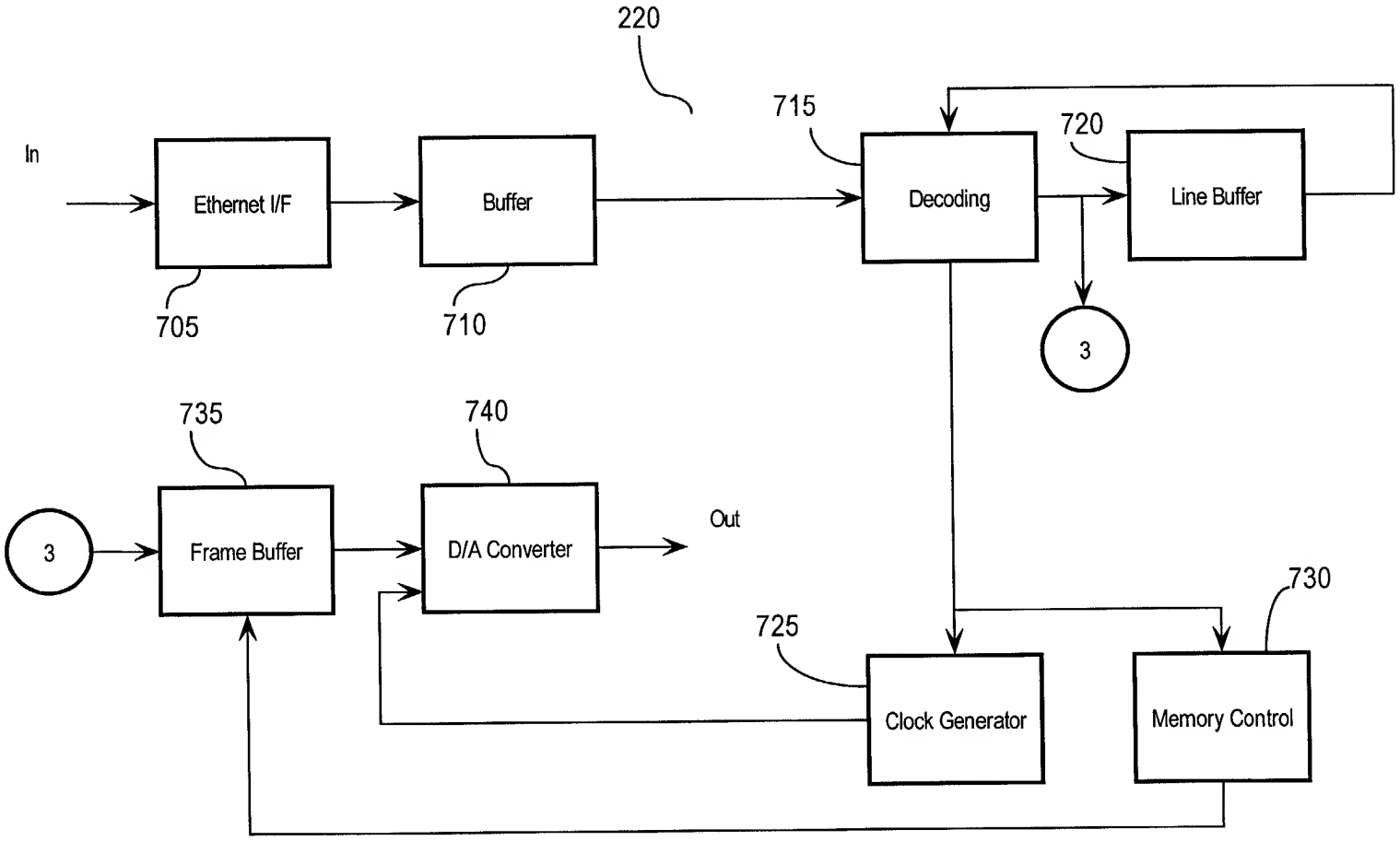

220
715
720
In
Ethernet I/F
Buffer
Decoding
Line Buffer
705
710
3
735
740
3
Frame Buffer
D/A Converter
Out
730
725
Clock Generator
Memory Control
Sync Circuitry

Fig. 7

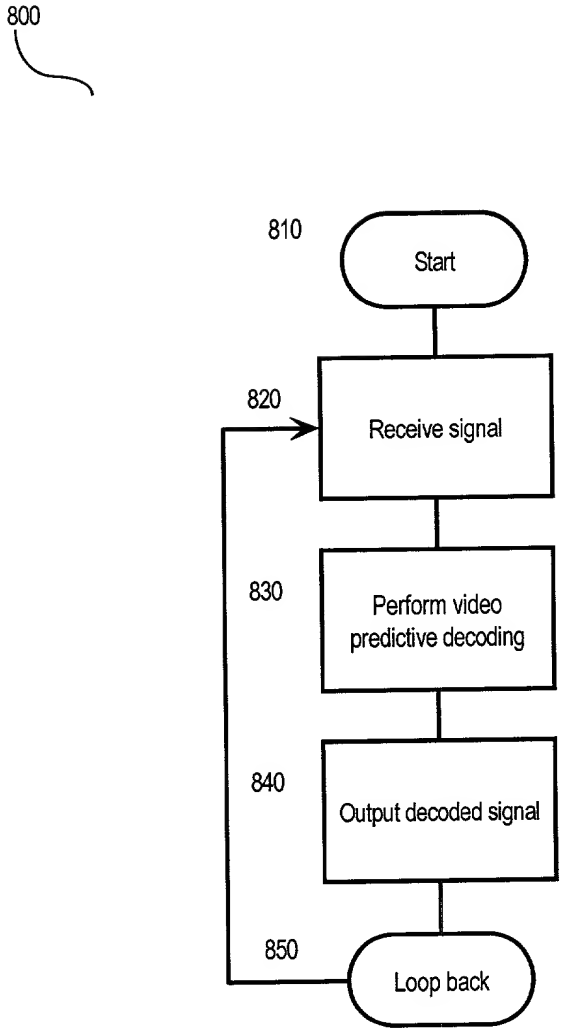

800
810
Start
820
Receive signal
830
Perform video predictive decoding
840
Output decoded signal
850
Loop back

Fig. 8

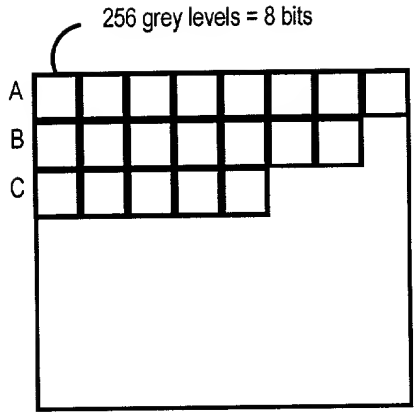


Fig. 9

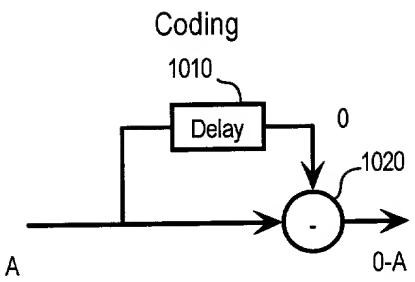


Fig. 10a

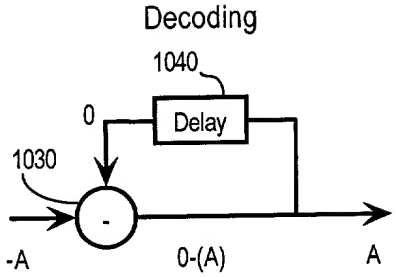


Fig. 10b

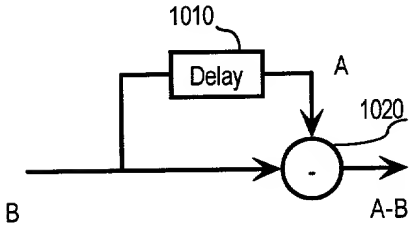


Fig. 10c

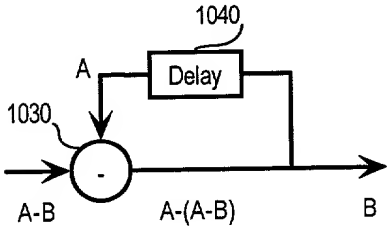


Fig. 10d

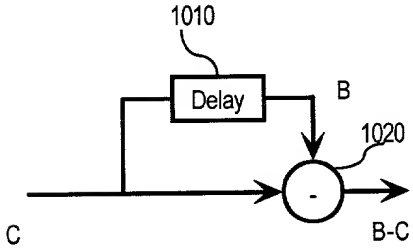


Fig. 10e

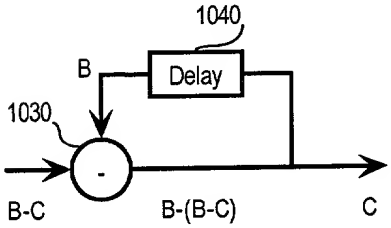


Fig. 10f

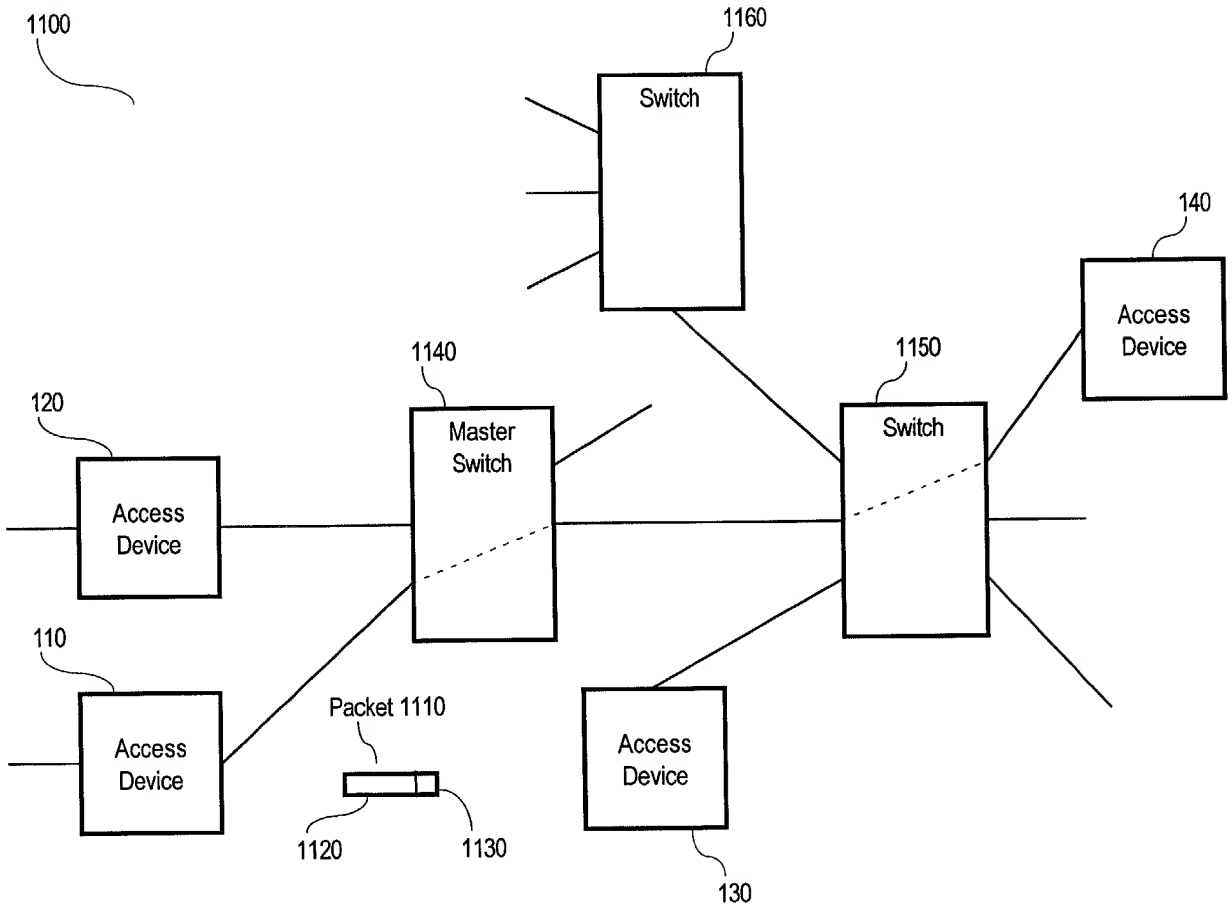

1100
1160
Switch
140
Access Device
1140
1150
120
Master Switch
Switch
Access Device
110
Packet 1110
Access Device
1120
1130
130

Fig. 11

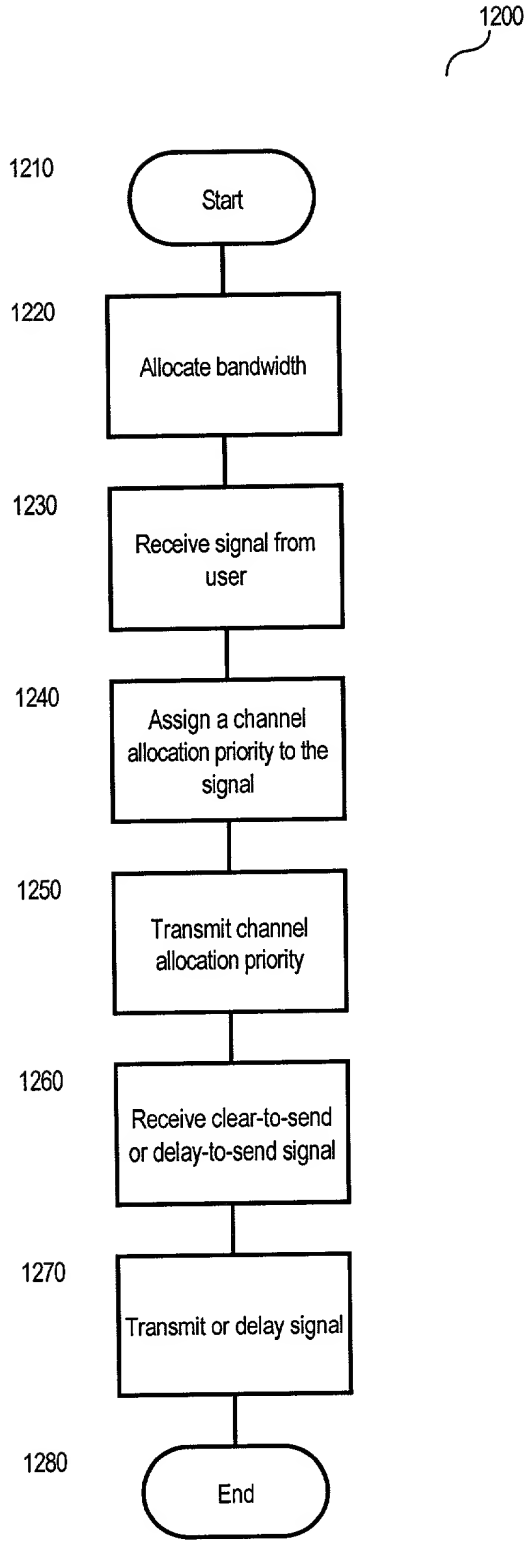

1200
1210
Start
1220
Allocate bandwidth
1230
Receive signal from user
1240
Assign a channel allocation priority to the signal
1250
Transmit channel allocation priority
1260
Receive clear-to-send or delay-to-send signal
1270
Transmit or delay signal
1280
End

Fig. 12

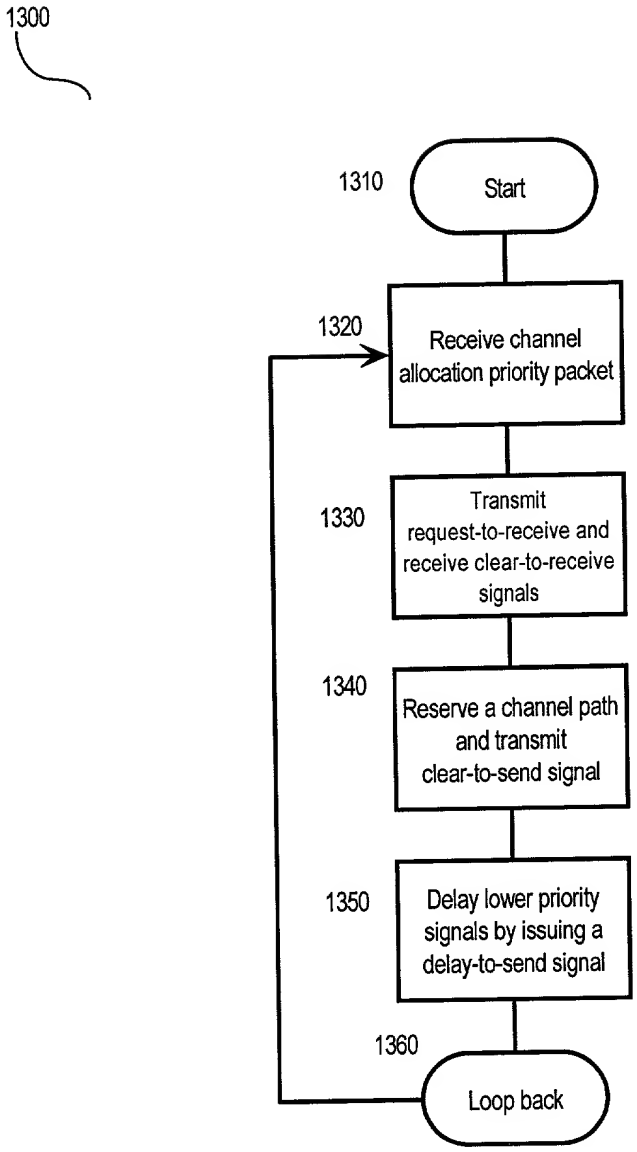

1300
1310
Start
1320
Receive channel allocation priority packet
1330
Transmit request-to-receive and receive clear-to-receive signals
1340
Reserve a channel path and transmit clear-to-send signal
1350
Delay lower priority signals by issuing a delay-to-send signal
1360
Loop back

Fig. 13